

CLAIMS

What is claimed is:

- 1 1. A printer, comprising:
- 2 (a) a first address bus;
- 3 (b) a second address bus;
- 4 (c) an address translation unit (ATU), coupled to the first and
- 5 second address buses, operable to translate virtual addresses received from at
- 6 least two bus masters connected to the first bus into physical memory
- 7 addresses.
- 1 2. The printer of claim 1, wherein the ATU is further operable
- 2 to transmit the physical address over the second bus.
- 1 3. The printer of claim 2, further comprising:
- 2 (d) a print engine coupled to the first address bus.
- 1 4. The printer of claim 3, further comprising:
- 2 (e) a central processing unit (CPU) coupled to the first address
- 3 bus.
- 1 5. The printer of claim 4, further comprising:
- 2 (f) a DMA controller coupled to the first address bus.
- 1 6. The printer of claim 5, further comprising:
- 2 (g) a memory coupled to the second address bus.
- 1 7. The printer of claim 6, wherein the CPU and the DMA
- 2 controller are both operable to transmit virtual addresses to the ATU over the
- 3 first address bus.
- 1 8. The printer of claim 7, wherein the ATU is operable to
- 2 translate the virtual addresses received from the CPU controller and the DMA

3 controller into physical addresses for addressing the memory and to then
4 transmit these physical addresses to the memory over the second address bus.

1 9. A printer , comprising:

2 (a) a DMA controller operable to generate virtual addresses;

3 (b) a CPU operable to generate virtual addresses; and

4 (c) an address translation unit operable to receive the virtual

5 addresses from both the DMA controller and the CPU and to translate the virtual
6 addresses into physical addresses.

1 10. The printer of claim 9, further comprising:

2 (d) a memory coupled to the address translation unit.

1 11. The printer of claim 10, wherein the address translation unit
2 is operable to transmit the physical addresses to the memory.

1 12. The printer of claim 11, further comprising:

2 (e) a virtual memory bus; and

3 (f) a physical bus; and

4 (g) wherein the DMA controller and the CPU is coupled to the

5 virtual memory bus and the memory is coupled to the physical bus and the

6 address translation unit is coupled to both the virtual memory bus and the

7 physical memory bus.

1 13. The printer of claim 12, further comprising:

2 (h) a print engine coupled to the virtual memory bus.

1 14. In a printer, including a CPU, a DMA controller, and a

2 memory, method of generating physical addresses for the memory, comprising:

3 (a) providing an address translation unit (ATU);

4 (b) the CPU transmitting a first plurality of virtual addresses to

5 the ATU; and

[illegible]

6 (c) the DMA controller transmitting a second plurality of virtual
7 addresses to the ATU.

1 15. The method of claim 14, further comprising
2 (d) the ATU generating physical addresses from the virtual
3 addresses received from the CPU.

1 16. The method of claim 15, further comprising:
2 (e) the ATU generating physical addresses from the virtual
3 addresses received from the DMA controller.

1 17. The method of claim 16, further comprising:
2 (f) The ATU transmitting the physical addresses generated in
3 step (d) to the memory.

1 18. The method of claim 16, further comprising:
2 (f) the ATU transmitting the physical addresses generated in
3 step (e) to the memory.

1 19. A computer, comprising:
2 (a) a DMA controller;
3 (b) a CPU; and
4 (c) an address translation unit operable to receive virtual
5 addresses from both the DMA controller and the CPU and to translate the virtual
6 addresses into physical addresses.

1 20. The computer, further comprising:
2 (d) a memory coupled to the address translation unit; and
3 wherein the address translation unit is operable to transmit the physical
4 addresses to the memory.